In re Patent Application of
KAUSHIK ET AL.
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In the Specification:

Please replace the paragraph beginning at page 7, paragraph 0030, with the following rewritten paragraph:

"[0030] A more detailed embodiment of an output buffer and control circuit according to the present invention will now be described with reference to FIGs. 6-8. Fig. 6 illustrates a CMOS output buffer, including a pre-driver 102, a pad driver circuit 100, a control circuit 101 for controlling ground bounce and an AND gate A1. The output buffer also includes IO PAD 103. One input of A1 is connected to configuration bit CB while other input is connected to NIN3 which is coming from pre driver 102. Output driver 100 includes PMOS P1 with it's drain connected to the output pad 103 and source connected to power supply VDD. Output driver 100 also includes NMOSs N1 and N2 with their drains connected to output pad 103 and their sources connected to C2. The NMOS transistors are sized in a binary-weighted sequence. C2 is connected to ground GND via parasitic inductor L1. PIN1 and NIN1 are coming from predriver 102 and connected to the gates of transistor P1 and N1 respectively. NIN3 is coming from predriver 102 which is connected to one of the inputs of AND gate A1. NIN2 is gate voltage for N2 coming from control circuit 101."

Please replace the paragraphs beginning at page 11, paragraphs 0037-0038, with the following rewritten paragraphs:

"[0037] Fig. 8 ~~3~~ shows the voltage waveforms at different nodes. NIN2 starts increasing from 0V at time T0. As N2

becomes ON ground bounce starts increasing. At time T1 V(C2) crosses the threshold level of N4. This will reduce the slew rate of NIN2. Reduction in the slew rate of NIN2 can be seen from time T1 to T2. Even with the reduction in slew rate ground bounce (V(C2)) still increasing. At time (T2-dt) G1 trips and makes N3 OFF. At time T2 voltage at line NIN2 starts falling because of N4. This reduces the current flowing through L1 because of which voltage at node C2 starts decreasing. At time (T2+dt) G1 again trips making N3 ON. NIN2 doesn't start increasing instantaneously as N3 has some delay and also N4 is still conducting to stop NIN2 from increasing. At T3 NIN2 starts increasing which again results in increase in the ground bounce. But this time the magnitude of voltage at V(C2) remains well below Vtrip(G1). The control circuit is working on feedback principle so it never allows ground bounce to cross Vmtp.

[0038] Secondly, under worst operating conditions magnitude of voltage at C2 is less than Vtrip(G1). The output of G1 always remains VDD and hence N3 always remains ON. During slow operating conditions its N4 which slightly reduces the slew rate at NIN2. The above explained circuitry not only controls the ground bounce but it also tries to equalize delays under different operating conditions. Under fast operating conditions as the bounce approaches Vmtp, N3 becomes OFF which controls the bounce from further increase. With N3 OFF and N4 ON, the voltage at NIN2 actually starts falling as shown in Fig. 8 ~~3~~. This reduces the current flowing through L1 because of which voltage at node C2 starts decreasing. This makes N4 less conducting. After a time 2dt N3 again turns ON but

voltage at NIN2 starts increasing only after a delay of T3-(T2+dt) as shown in Fig. 8 ~~3~~ whereas under slow operating conditions N3 is always ON and a slight reduction in the slew rate by N4 is sufficient to control the bounce. Thus in best operating conditions the bounce is controlled by actually decreasing the voltage at NIN2 whereas in worst operating conditions the bounce is controlled by slightly reducing the slew rate of voltage at NIN2."